REMARKS

In sections 1-2 of the Office Action, claims 1-3, 7-12 and 14-18 are rejected under 35 USC 103(a) as being unpatentable over Polgreen et al. (US Patent No. 5,465,189) in view of Bez et al. (US Patent No. 6,071,778). These rejections are respectfully traversed.

Polgreen et al. and Bez et al., standing alone or in combination, fail to disclose, teach, or suggest, *inter alia*, the following features recited by claim 1 of the present application:

"a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased, wherein at least one of the isolated islands is completely surrounded by the first doped region".

Polgreen et al. discloses a semiconductor controller rectifier used to provide on-chip protection against ESD stress applied at the input, output and power supply pins. Polgreen et al., however, nowhere teaches a plurality of isolated islands distributed in the first doped region ... wherein at least one of the isolated islands is completely surrounded by the first doped region", as recited by claim 1 of the present application.

In section 2 of the Office Action, the Examiner admits that Polgreen et al. fails to disclose the features quoted above. However, he asserts that Bez et al. teaches a plurality of isolated islands 65 distributed in the doped region (6, 7 and 14) and that it would have been obvious to obtain the

claimed invention by incorporate the teaching of Bez et al into the device taught by Polgreen et al. because it isolates the diffusion areas in the **ESD device**. The Applicants disagree.

First, Bez et al. teaches a memory device rather than an ESD device as asserted by the Examiner. Further, as shown in Figs. 2-5 showing the cross-sectional views of the portion of memory cell array of Fig.1, the field oxides 65 are not distributed in the first doped region 6 and 14 and are completely surrounded by the first doped region 6 and 14. As cited on lines 65~67 in column 5, the regions 65 of thick field oxide are formed to define the active areas for the doped regions 6, 7 and 14 rather than isolate diffusion areas in the ESD device as asserted by the Examiner. As field oxide 65 are used to define active area, the field oxides 65 are impossible to be distributed in the first doped region 6, 7 and 14 in the active area and completely surrounded by the first doped region 6, 7 and 14. Even in Fig. 3 of Bez, the field oxides 65 are across the doped region 14 rather than completely surrounded by the doped region 14. Where does Bez suggest that field oxide can be distributed in the active area and completely surrounded by the active area?

Furthermore, Bez et al. and Polgreen et al. do not teach distributing isolated islands to a doped region to increase the resistance of the doped regions in the ESD device. Thus, there is no motivation or suggestion that the isolated islands are distributed in the first doped region such that the resistance of the first doped region is increased as claimed in claims 1 and 12. Accordingly, the prior art references (or references when combined) do not teach or suggest all the claimed limitations in claim 1.

Similarly, claim 12 recites, in part, "a plurality of isolated islands, formed between the contact region and the first side of the gate structure in the first doped region, resulting in increased resistance of the first doped region, wherein at least one of the isolated islands is completely surrounded by the first doped region". Claim 12 is patentable for the same reasons as claim 1. Moreover, as cited in claim 12, the MOS has a gate structure, first and second doped regions and a plurality of isolated islands, wherein the islands are distributed in the first doped region and completely surrounded by the first doped region of the MOS. Bez et al and Polgreen et al, however, do not teach distributing isolated islands in a first doped region of a MOS and completely surrounded by the first doped region to increase the resistance of the doped regions in the ESD device.

Due to the reasons stated above, the Applicants respectfully submit that claim 1 and claim 12 are patentable. Claims 2-3, 7-11 and 14-18 are also patentable, at least by virtue of their dependency from claim 1 or claim 12.

The Applicants have attempted to address all of the issues raised by the Examiner in the Office Action as the Applicants understand them. It is believed that the application is now in condition for allowance. If any point requires further explanation, the Examiner is invited to telephone Troy Cai at (323) 934-2300 or e-mail Troy Cai at tcai@ladasparry.com.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account No. 12-0415. In particular, if this response is not timely filed, then the Commissioner is

authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

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Troy Guangyu Cai

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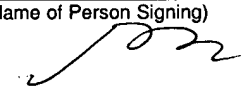

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8/26/04

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Respectfully submitted,

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